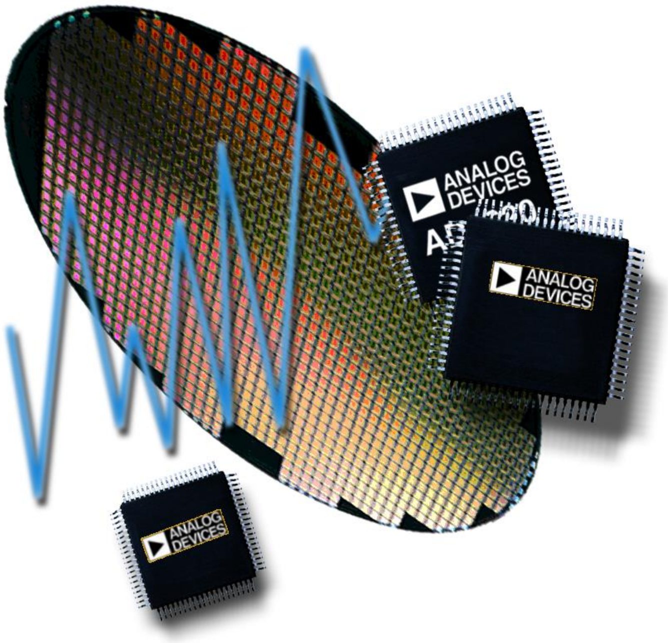
ANALOG
DEVICES



Reliability Report

Report Title: **27x27mm PBGA at AEG Qualification**

Report Number: **20197**

Revision: **A**

Date: **9 August 2023**

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADSP-TS101S product in a 625-BGA package. The ADSP-TS101S TigerSHARC® processor is an ultrahigh performance, Static Superscalar$^{TM\ \dagger}$ processor optimized for large signal processing tasks and communications infrastructure. The DSP combines very wide memory widths with dual computation blocks—supporting 32- and 40-bit floating-point and 8-, 16-, 32-, and 64-bit fixed-point processing—to set a new standard of performance for digital signal processors.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	ADSP-TS101S
Die Id	TMH742 D
Die Size (mm)	10.36 x 10.52
Wafer Fabrication Site	E_TSMC1212
Wafer Fabrication Process	0.13um CMOS
Die Substrate	Si
Metallization / # Layers	AlCu(0.5%)/8
Polyimide	Yes
Passivation	undoped-oxide/SiN

Package/Assembly Product Characteristics

Table 2: Package/Assembly Product Characteristics

Product Characteristics	Product(s) to be qualified
Generic/Root Part #	ADSP-TS101S
Package	625-BGA
Body Size (mm)	27.00 x 27.00 x 1.73
Assembly Location	ASE (AEG)
MSL/Peak Reflow Temperature(°C)	3 / 260°C
Mold Compound	Hitachi CEL9750ZHF10AK
Die Attach	Ablestik 2100AC conductive
Terminal Finish Composition	96.5Sn_3.0Ag_0.5Cu
Wire Bond Material/Diameter (mils)	4N Gold / 1.20

Package/Assembly Test Results

Table 3: Package/Assembly Test Results

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
High Temperature Storage Life (HTSL)[1]	JESD22-A103	150°C, 1,000 Hours	ADSP-TS101S	Q20197.1.HS1	0/32
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1,2]	JESD22-A110	110C 85%RH 17.7 psia, Biased, P264	ADSP-TS101S	Q20197.1.HA1	0/32
				Q20197.2.HA2	0/32
				Q20197.3.HA3	0/32
Solder Heat Resistance (SHR)[1]	J-STD-020	MSL-3	ADSP-TS101S	Q20197.1.SH1	0/11
				Q20197.2.SH2	0/11
				Q20197.3.SH3	0/11
Temperature Cycling (TC)[1,2]	JESD22-A104	-55°C/+125°C, 1,000 Cycles	ADSP-TS101S	Q20197.1.TC1	0/32
				Q20197.2.TC2	0/32
				Q20197.3.TC3	0/32
Unbiased HAST (UHST)[1,2]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADSP-TS101S	Q20197.1.UH1	0/32
				Q20197.2.UH2	0/32
				Q20197.3.UH3	0/32

[1] Electrical test was performed at Cold temperature.

[2] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 4: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	ADSP-TS101S	625-BGA	JS-002	1Ω, Cpkg	±250V[1]	C1

[1] Corner balls passed 2000V ESD FICDM (highest level tested).

Latch-up testing was not performed.

Approvals

Reliability Engineer: Lucille Jordan